

## 40CH Segment/Common Driver

### ■ Functions:

- Dot matrix LCD driver with two 20 channel outputs
- Selectable function to use common/segment drivers simultaneously
- Bias voltage (V1 ~ V6)
- Input/output signals
  - Input : Serial display data and control pulse from controller IC
  - Output : 20 X 2 channels waveform for LCD driving

### ■ Features:

- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (V<sub>0</sub>~V<sub>SS</sub>) : 3V ~ 7.2V
- 64 Pin QFP package and bare chip available

### ■ Description:

**RW1060** is a segment/common driver for dot matrix type LCD display. It features 40 channels with 20 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

The **RW1060** can convert serial data received from a LCD controller, such as **RW1068** and **RW1067**, into parallel data and send out LCD

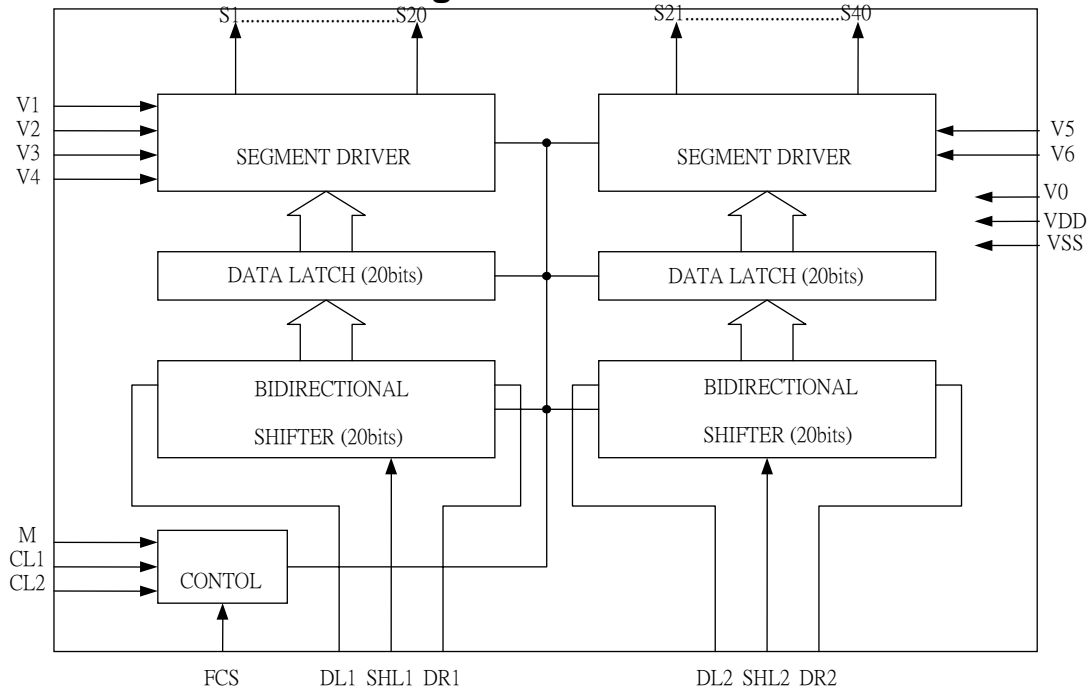
driving waveforms to the LCD panel. The **RW1060** is designed for general-purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment/common driver.

The **RW1060** has pin function compatibility with the KS0065B that allows the user easily to replace it with a **RW1060**.



## 40CH Segment/Common Driver

### Functional Block Diagram



### Pad Arrangement

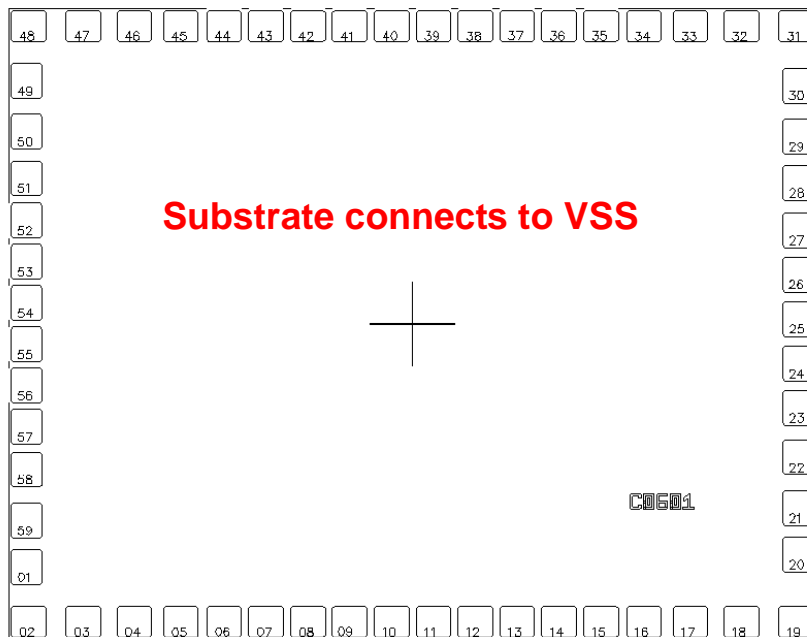
Chip size: 1907um x 1511um

Chip thickness: 482.6 um

PAD Pitch: 99 um ~ 130 um

PAD Size: PIN 1、20~30、49~59: 82.3um X 91um

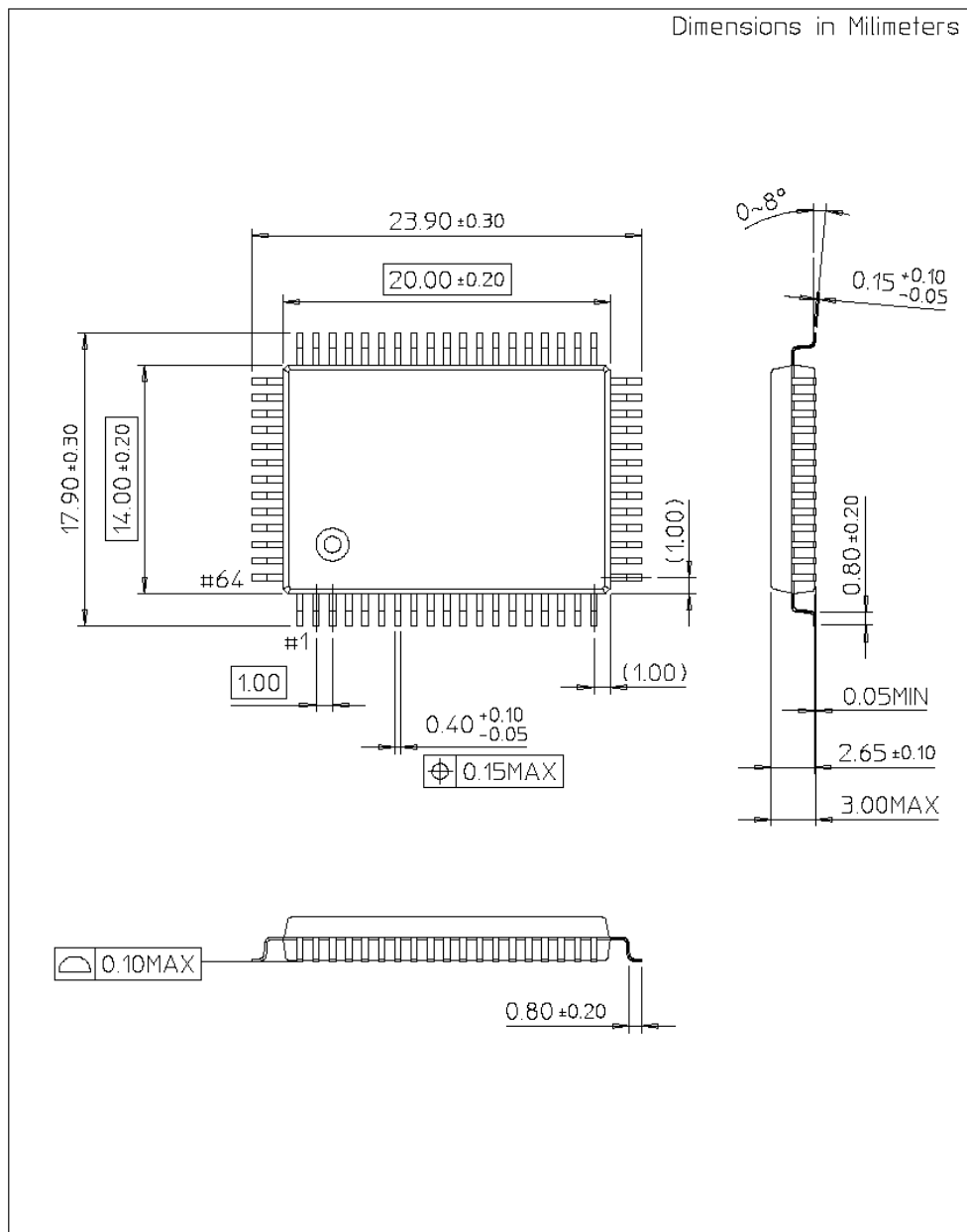
PIN 2~19、31~48: 91um X 82.3um



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### ■ Package Dimensions

64-QFP-1420F





## 40CH Segment/Common Driver

### ■ Pad Name and Coordinates

Pad No.	Pad Name	X	Y
1	V0	-912.2	-574.45
2	CL1	-907.85	-704.45
3	CL2	-777.85	-704.45
4	VSS	-657.85	-704.45
5	DL1	-547.85	-704.45
6	DR1	-445.15	-704.45
7	DL2	-346.15	-704.45
8	DR2	-247.15	-704.45
9	M	-148.15	-704.45
10	SHL1	-49.15	-704.45
11	SHL2	49.85	-704.45
12	FCS	148.85	-704.45
13	V1	247.85	-704.45
14	V2	346.85	-704.45
15	V3	445.85	-704.45
16	V4	547.85	-704.45
17	V5	657.85	-704.45
18	V6	777.85	-704.45
19	S[40]	907.85	-704.45
20	S[39]	912.2	-545.1
21	S[38]	912.2	-435.1
22	S[37]	912.2	-315.1
23	S[36]	912.2	-198.4
24	S[35]	912.2	-93.4
25	S[30]	912.2	11.6
26	S[31]	912.2	116.6
27	S[32]	912.2	221.6
28	S[33]	912.2	333.1
29	S[34]	912.2	443.1
30	S[29]	912.2	563.1

Pad No.	Pad Name	X	Y
31	S[28]	907.85	704.25
32	S[27]	777.85	704.3
33	S[26]	657.85	704.3
34	S[25]	547.85	704.3
35	S[24]	445.85	704.3
36	S[23]	346.85	704.3
37	S[22]	247.85	704.3
38	S[21]	148.85	704.3
39	S[20]	49.85	704.3
40	S[19]	-49.15	704.3
41	S[18]	-148.15	704.3
42	S[17]	-247.15	704.3
43	S[16]	-346.15	704.3
44	S[15]	-445.15	704.3
45	S[14]	-547.85	704.3
46	S[13]	-657.85	704.3
47	S[12]	-777.85	704.3
48	S[9]	-907.85	704.25
49	S[10]	-912.2	574.25
50	S[11]	-912.2	454.25
51	S[8]	-912.2	344.25
52	S[7]	-912.2	244.25
53	VDD	-912.2	146.75
54	S[6]	-912.2	49.25
55	S[5]	-912.2	-48.25
56	S[4]	-912.2	-145.75
57	S[3]	-912.2	-243.25
58	S[2]	-912.2	-344.45
59	S[1]	-912.2	-464.45

## 40CH Segment/Common Driver

### ■ Pin Description:

Pin Name	Purpose	Description	I/O
VDD	POWER	for logic	N/A
VSS	GROUND	for logic	N/A
V0	LCD power	for LCD driving voltage(positive voltage)	N/A
V1 V2	LCD output	used as select voltage level(positive voltage)	I
V3 V4	LCD output	Used as non select voltage level for Part I (positive voltage)	I
V5 V6	LCD output	Used as non select voltage level for Part II (positive voltage)	I
S[1]-S[20]	segment	LCD driver output for part 1	O
SHL1	direction	direction control for part 1 segments	I
DL1, DR1	data in /out	If SHL1 = 1 then DL1=out, DR1=in If SHL1 = 0 then DL1=in, DR1=out	I/O
S[21]-S[40]	segment	LCD driver output for part 2	O
SHL2	direction	direction control for part 2 segments	I
DL2, DR2	data in/out	If SHL2 = 1 then DL2=out, DR2=in If SHL2 = 0 then DL2=in, DR2=out	I/O
M	alternation	Alternate the LCD driving waveform	I
CL1	latch clock	latch the data after shift is completed	I
CL2	shift clock	shift the data into the segments	I
FCS	mode selection	mode select signal for Part II	I

## 40CH Segment/Common Driver

### ■ Functional Description:

#### Shift Registers and Data I/O

The **RW1060** supplies two sets of shift register, which controls the shift direction by SHL1 & SHL2. The DL1, DR1, DL2 and DR2 are data input or output option function.









Shift Direction of Channel 1			
SHL1	Shift Direction	DL1	DR1
0	S[1] → S[20]	IN	OUT
1	S[20] → S[1]	OUT	IN

Shift Direction of Channel 2			
SHL2	Shift Direction	DL2	DR2
0	S[21] → S[40]	IN	OUT
1	S[40] → S[21]	OUT	IN

#### Clock and Mode Selection

In channel 1 part, the CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

In channel 2 parts, the CL1 and CL2 is the clock to latch or shift data on the falling or rising edge which is depend on FCS value. When FCS is low, the channel 2 function is the same as channel 1 as a segment driver. When FCS is high, the channel 2 function will become a common driver. Detail functions are show in the following table:

FCS	Clock Edge	Channel 1	Channel 2	
0	CL1		Latch data	Latch Data
			----	----
	CL2		Shift data	Shift data
			----	----
1	CL1		Latch data	----
			----	Shift data
	CL2		Shift data	----
			----	Latch data

**40CH Segment/Common Driver****■ LCD Output Waveform**

The output levels of channel1 and channel2 are decided by the combination of FCS, M, and latched data. Refer to the following table:

<b>FCS</b>	<b>Latched Data</b>	<b>M</b>	<b>Channel 1</b>	<b>Channel 2</b>
1	1	1	V1	V2
		0	V2	V1
	0	1	V3	V6
		0	V4	V5
0	1	1	V1	V1
		0	V2	V2
	0	1	V3	V5
		0	V4	V6

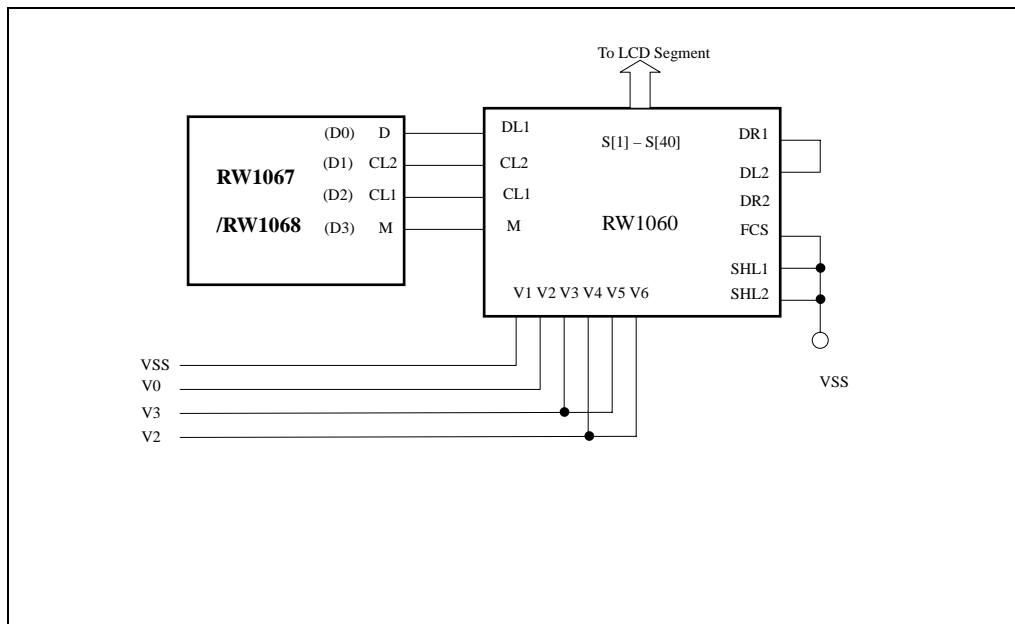
Note:

To use the same function of channel 1 and channel 2 as a segment driver, V3 and V5, V4 and V6 need to short respectively.

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### Both Channels 1 and 2 used as segment drivers (FCS=0)

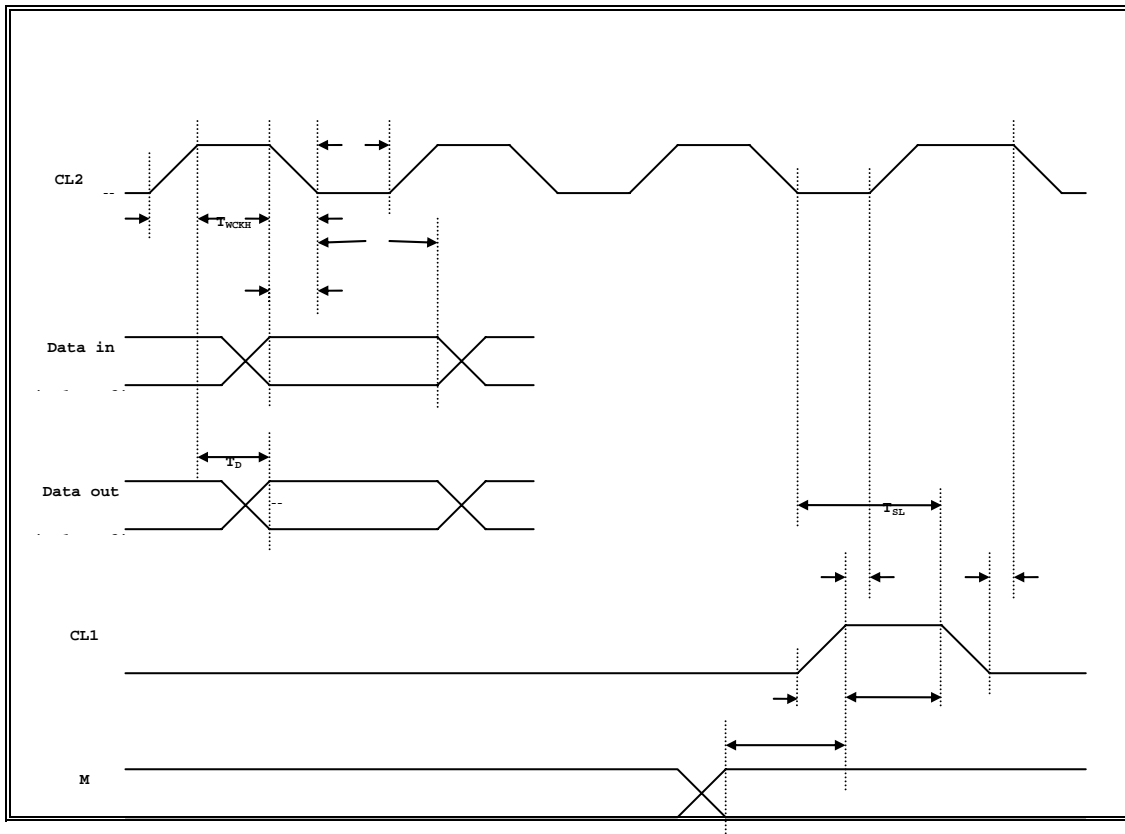
When both channels 1 and 2 of the **RW1060** are used as segment drivers, they will shift data on the falling edge of CL2 and latch data on the falling edge of CL1. V3&V5, V4&V6 are shorted in the application circuit as shown in the following figure.



※ Power down function is reserved in RW1067+RW1060 configuration

## 40CH Segment/Common Driver

### ■ Timing Characteristics



## 40CH Segment/Common Driver

### ■ D.C Characteristics:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Applicable pin
VDD	Operating Voltage	-	2.7	-	5.5	V	-
V0	Driver Supply Voltage	V0-VSS	3	-	7.2	V	-
VIH	Input High Voltage	-	0.7 VDD	-	VDD	V	CL1,CL2,M,SHL1,S HL2 DL1,DL2,DR1,DR2
VIL	Input Low Voltage	-	0	-	0.3 VDD	V	
ILKG	Input Leakage Current	VIN = 0 ~ VDD	-5	-	5	uA	
VOH	Output High Voltage	IOH = -0.4mA	VDD -0.4	-	-	V	DL1,DL2,DR1,DR2 V1~V6, S[1]~S[40]
VOL	Output Low Voltage	IOL = +0.4mA	-	-	0.4	V	
IDD	Operating Current	FCL2 = 400KHZ	-	100	300	uA	V0,VSS
IV	Leakage Current	VIN = V0 ~ VSS	-10	-	10	uA	V1 ~ V6

### ■ A.C Characteristics:

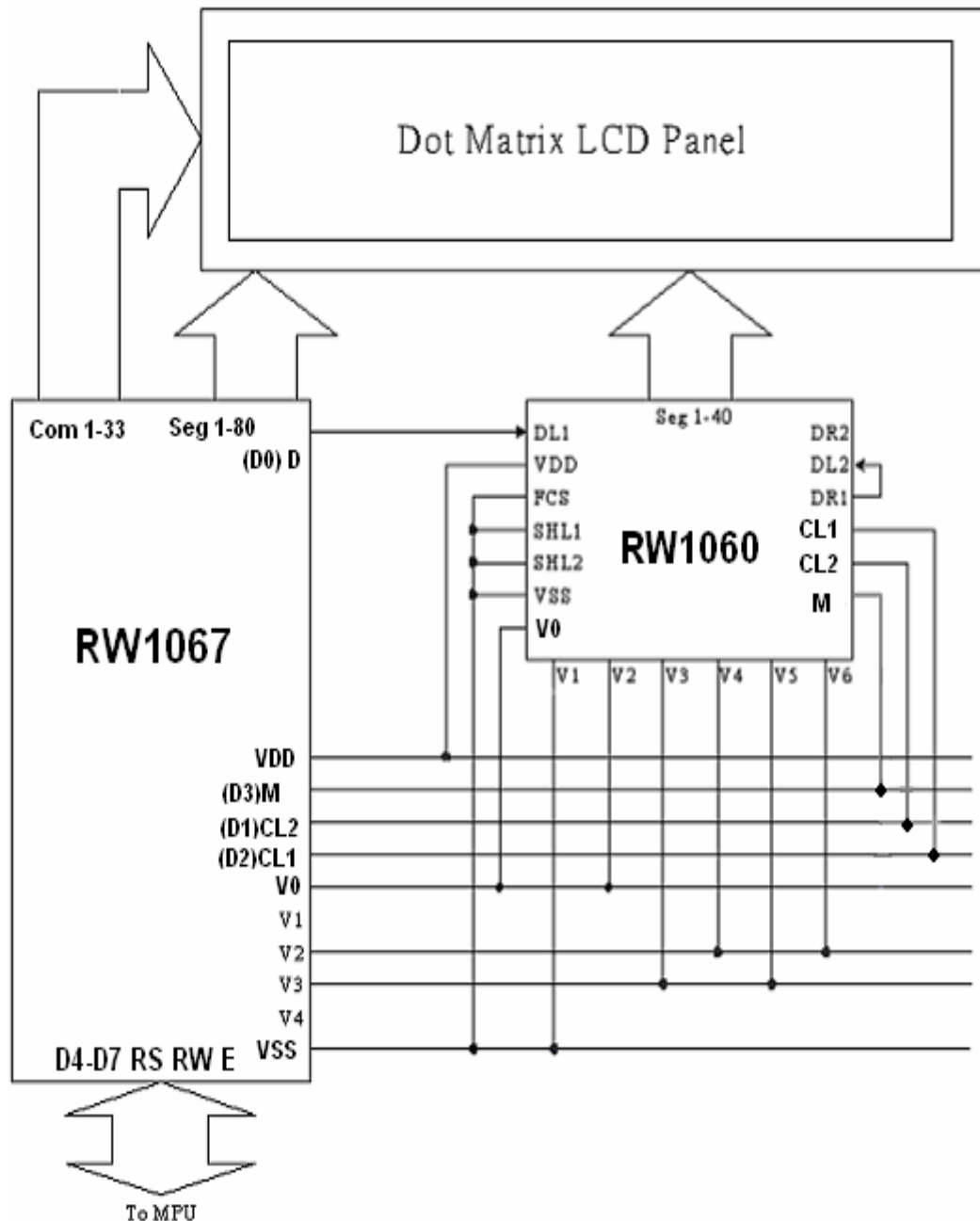
Symbol	Parameter	Test Condition	Min.	Max.	Unit	Applicable pin
FCL	Data Shift Frequency	-	-	400	KHZ	CL2
TWCKH	Clock High Level Width	-	800	-	ns	CL1,CL2
TWCKL	Clock Low Level Width	-	800	-	ns	CL2
TSL	Clock Set-up Time	CL2 → CL1	500	-	ns	CL1,CL2
TLS	Clock Set-up Time	CL1 → CL2	500	-	ns	CL1,CL2
TR/TF	Clock Rise/Fall Time	-	-	200	ns	CL1,CL2
TSU	Data Set-up Time	-	300	-	ns	DL1,DL2,DR1,DR2
TDH	Data Hold Time	-	300	-	ns	DL1,DL2,DR1,DR2
TD	Data Delay Time	CL = 15 PF	-	500	ns	DL1,DL2,DR1,DR2

### ■ Maximum Absolute Ratings:

Symbol	Parameters	Min.	Max.	Unit
VDD	Supply Voltage	-0.3	5.5	V
TOPR	Operating Temperature	-40	90	°C
TSTG	Storage Temperature	-55	125	°C

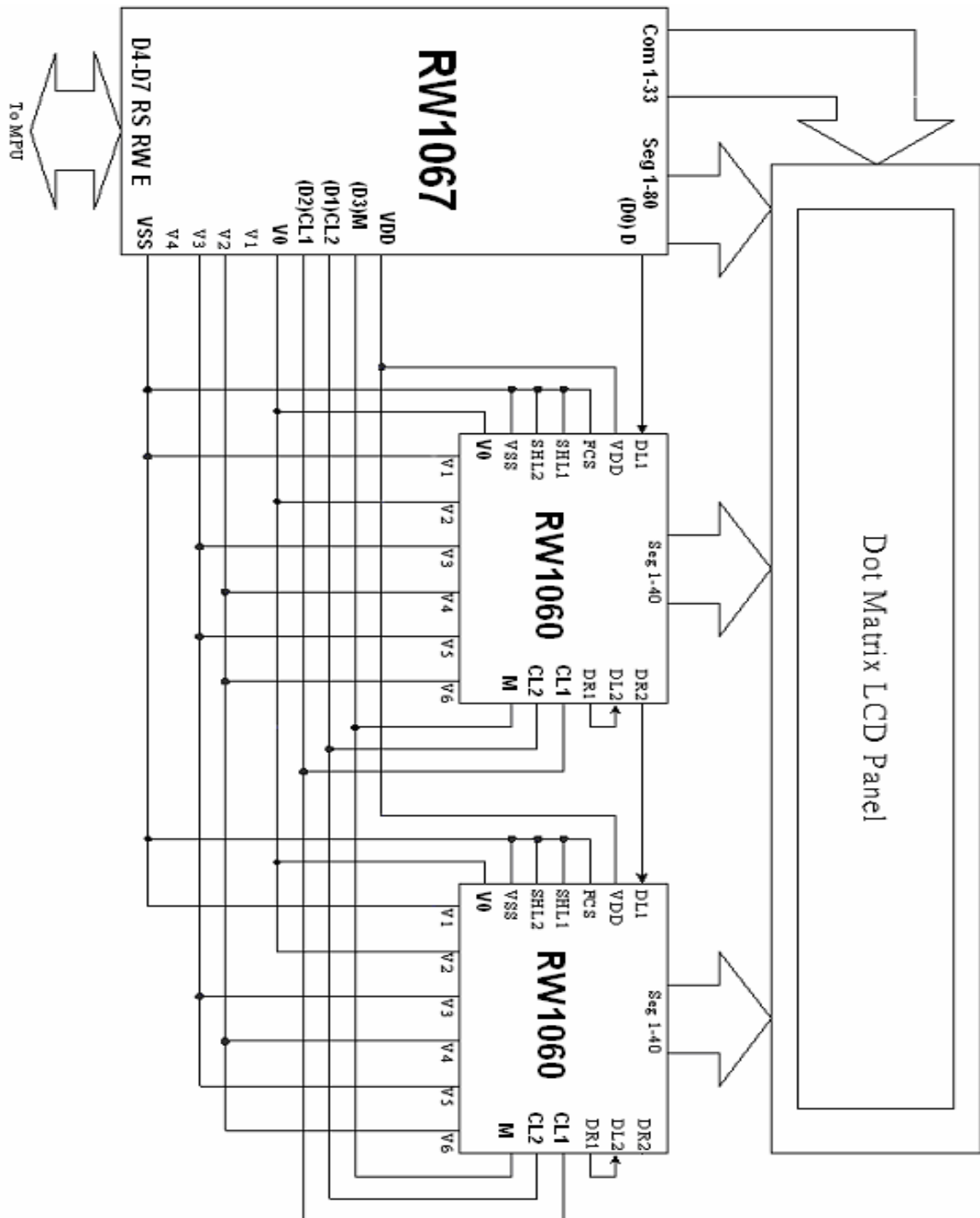
## 40CH Segment/Common Driver

- RW1067 Application Circuit: (4Line x 20Channels) – RW1060\*1**  
 RW1067+RW1060 mode is not available in 8 bit parallel interface, only 4 bit parallel interface, SPI-3/SPI-4 can be used for RW1067+RW1060 mode.  
 Power down function is reserved in RW1067+RW1060 configuration.



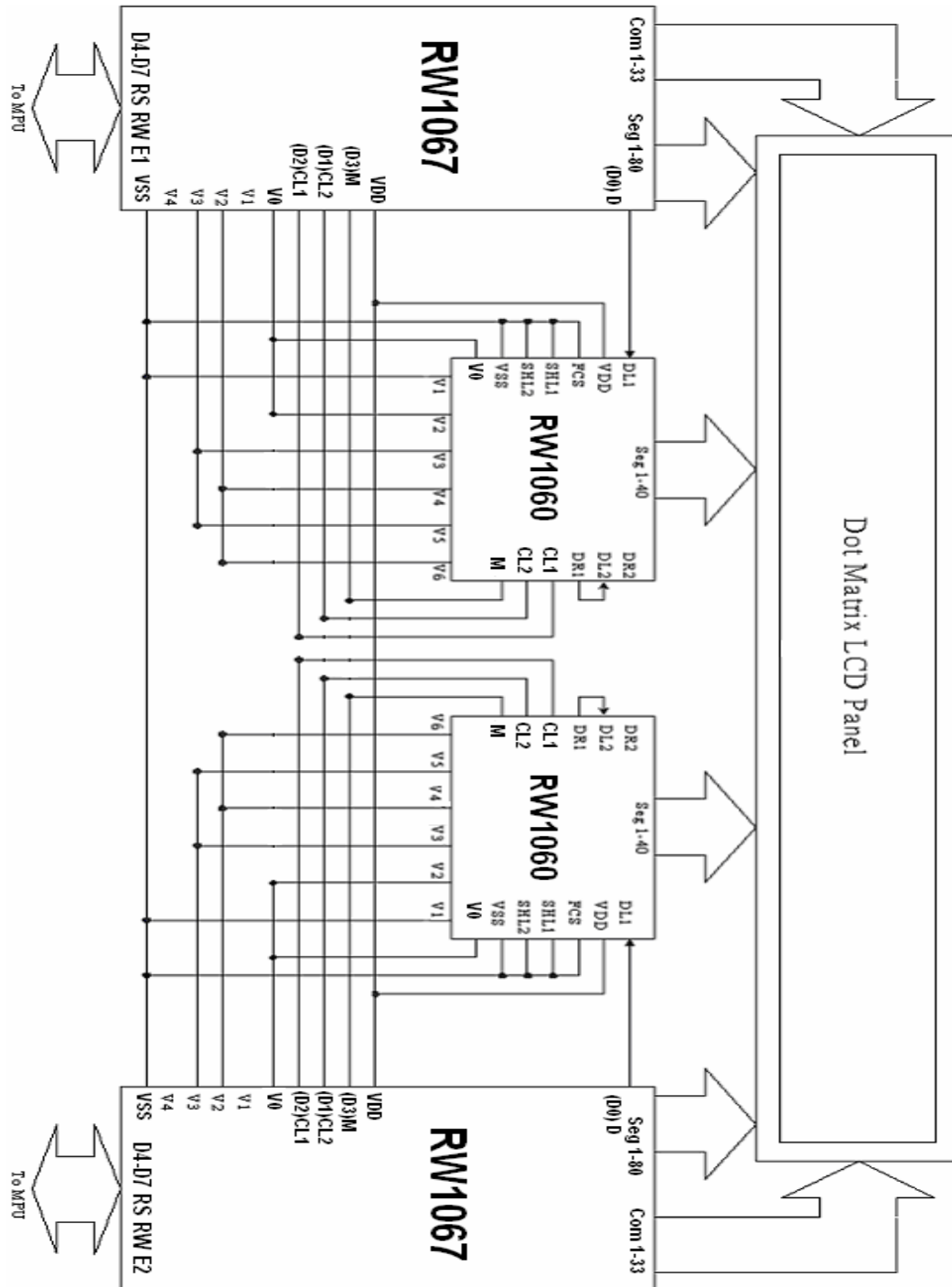
## 40CH Segment/Common Driver

- RW1067 Application Circuit: (2Line x 32Channels) – RW1060\*2**  
 (2Line x 24Channels – RW1060\*1, 2Line x 40Channels – RW1060\*3)  
 RW1067+RW1060\*2 mode is not available in 8 bit parallel interface, only 4 bit parallel interface, SPI-3/SPI-4 can be used for RW1067+RW1060 mode.  
 Power down function is reserved in RW1067+RW1060 configuration.



## 40CH Segment/Common Driver

- RW1067 Application Circuit: (4Line x 40Channels)**  
 RW1067\*2+RW1060\*2 mode is not available in 8 bit parallel interface, only 4 bit parallel interface, SPI-3/SPI-4 can be used for RW1067+RW1060 mode.  
 Power down function is reserved in RW1067+RW1060 configuration.



## 40CH Segment/Common Driver

- RW1068 Application Circuit: (2Line x 10Character) – RW1060\*1**  
 (2Line x 13 Character – RW1060\*2, 2Line x 17Character – RW1060\*3,  
 2Line x 20 Character – RW1060\*4)

RW1068+RW1060 mode is not available in 8 bit parallel interface, only 4 bit parallel interface, SPI-3/SPI-4 can be used for RW1067+RW1060 mode.

